PATENT
Docket No.: M4065.0127/P127-A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kie Ahn et al.

Serial No.: Not Yet Assigned

Group Art Unit: 2815

Filed: September 12, 2000

Examiner: Not Yet Assigned

For: SILICON MULTI-CHIP MODULE PACKAGING WITH INTEGRATED PASSIVE COMPONENTS AND METHOD OF MAKING

Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT (IDS)

Dear Sir:

Pursuant to 37 C.F.R. 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

x 1. This Information Disclosure Statement is being filed within three months of the U.S. filing date OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. 1.491, OR before the mailing date of a first Office Action on the merits, whichever event occurs last. No certification or fee is required. 37 C.F.R. 1.97(b).

___ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage, AND after the mailing date of the first Office Action on the merits, whichever occurs first, but before the mailing date of a Final Rejection or Notice of Allowance. 37 C.F.R. 1.97(c).

___ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. 1.97(e)(1).

___ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. 1.97(e)(2).

___ c. Attached is our check in the amount of in payment of the fee under 37 C.F.R. 1.17(p). Please charge any fee deficiencies, or credit any overpayment, to Deposit Account No. 4 - 1073 as needed to ensure consideration of the Information Disclosure Statement. Two duplicate copies of this paper are attached.

___ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage, AND after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Applicant(s) hereby petition(s) that the Information Disclosure Statement be considered. Attached is our check in the amount of in payment of the petition fee under 37 C.F.R. 1.17(i)(1). Please credit or debit Deposit Account No. 4 - 1073 as needed to ensure consideration of the Information Disclosure Statement. Two duplicate copies of this paper are attached.

___ a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. 1.97(e)(1).

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___ 4. Translations of the non-English language references are enclosed.
___ Full
___ Partial
___ Summary/abstract

_X_ 5. A copy of the references can be found in U.S. Patent Application No. 09/241,061.

Dated: September 12, 2000

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION	Docket Number	Application Number
	M4065.0127/P127-A	Not Yet Assigned
	Applicant(s)	
	Kie Y. Ahn et al.	
	Filing Date	Group Art Unit
	September 12, 2000	2815

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A	5,770,476	6/23/98	Stone	438	106	5/15/97
	B	5,530,288	6/25/96	Stone	257	700	10/12/94
	C	5,539,241	7/23/96	Abidi et al.	257	531	2/15/95
	D	5,564,617	10/15/96	Degani et al.	228	6.2	6/7/95
	E	5,674,785	10/7/97	Akram et al.	437	217	11/27/95
	F	5,688,711	11/18/97	Person et al.	437	60	5/10/96

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translations YES	Translations NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	G	Burns; "Applications for GaAs and Silicon Integrated Circuits in Next Generation Wireless Communication System"; IEEE Journal of Solid-State Circuits, Vol. 30, No. 10, October 1995; pg. 1088-1095.
	H	Van Tuyl et al.; "A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits"; IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-30, No. 7, July 1982; pg. 935-942.
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	J	Chang et al.; "Large Suspended Inductors on Silicon and Their Use in a 2-μm CMOS RF Amplifier"; IEEE Electron Devices Letters, Vol. 14, No. 5, May 1993; pg. 246-248.
	K	Burghartz et al.; "Multilevel-Spiral Inductors Using VLSI Interconnect Technology"; IEEE Electron Devices Letters, Vol. 17, No. 9, September 1996; pg. 428-430.
	L	Burghartz et al.; "Integrated RF and Microwave Components in BiCMOS Technology"; IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996; pg. 1559-1570.
	M	Craninckx et al.; "A 1.8-GHz Low-Phase-Noise Spiral-LC CMOS VCO"; IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1996; pg. 30-31.
	N	Pieters et al.; "Spiral Inductors Integrated in MCM-D using the Design Space Concept"; IEEE International Conference on Multichip Modules and High Density Packaging, 1998; pg. 478-483.
	O	Samber et al.; "Low-Complexity MCM-D Technology with Integrated Passives for High Frequency Applications"; IEEE International Conference on Multichip Modules and High Density Packaging, 1998; pg. 285-290.
	P	Hartung; "Integrated Passive Components in MCM-Si Technology and their Applications in RF-Systems"; IEEE International Conference on Multichip Modules and High Density Packaging, 1998; pg. 256-261.
	Q	Hitko et al.; "A 1V, 5mW, 1.8GHz, Balanced Voltage-Controlled Oscillator with an Integrated Resonator"; Proc. Symp. on Low Power Electronics and Design, Monterey CA, 1997; pg. 46-51.
	R	Ahrens et al.; "A 1.4-GHz 3-mW CMOS LC Low Phase Noise VCO Using Tapped Bond Wire Inductances"; Proc. Symp. on Low Power Electronics and Design, Monterey CA, 1998; pg. 16-19.
	S	Saia et al.; "Thin Film Passive Elements on Polyimide Film"; IEEE International Conference on Multichip Modules and High Density Packaging, 1998; pg. 349-353.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.